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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/763,733 | 01/22/2004 | Peter John McElheny | A1167 | 7320 |

45851 7590 03/29/2006

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| EXAMINER | |
|---|---|
| KIK, PHALLAKA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 03/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/763,733 | MCELHENY, PETER JOHN | |
| | Examiner | Art Unit | |
| | Phallaka Kik | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action responds to the Applicant's amendment and drawings filed on 2/9/2006. Claims 1-21 are pending, wherein claims 1,3-4,17,18,21 have been amended.

### *Drawings*

2. The drawings were received on 2/9/2006. These drawings are approved by the Examiner.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-2,5,7,13-14,16,21** are rejected under 35 U.S.C. 102(e) as being anticipated by **Anderson et al.** (U.S. Patent No. 6,993,737).

As per **claims 1,7,14,21**, the generation of the configuration data for the programmable logic device using the logic design system that takes into account power consumption due to gate leak effects is summarized in col. 2, lines 30-59, wherein the leakage power being reduced includes gate leak as further described in col. 4, lines 26-

35, for which the modification being applied (see Fig. 3) so that components/signals are configured in the programmable logic devices to operate in the low power ranges based on the probability of the signals being high or low, using the generated configuration data is further described in col. 7, line 56 to col. 8, line 8, wherein the ability for the designer to specify the desired logic design using the logic design system is within the scope of the prior art, being necessary to allow the design (i.e., containing the particular signals and components) to be analyzed and to be modified that takes into consideration gate power consumption, wherein the computer readable medium, computing equipment, instructions are also described in col. 8, line 57 to col. 9, line 14.

As per **claims 2,5,13,** all of the elements of claims 1,7, from which the respective claims depend, are discussed in the rejections of claims 1 and 7 above, wherein the further limitation in which the type of signals information being gathered either from the logic designer and/or generated automatically is also part of software tools and techniques available for analyzing the signals (see col. 5, lines 8-36).

As per **claim 16**, all of the elements of claim 14, from which the claim depends, are discussed in the rejection of claim 14, wherein the further computing equipment being configured to perform logical synthesis and optimization of the logic design is also described in col. col. 8, lines 1-8.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 3-4,6,8,10-12,17-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Anderson et al.** (U.S. Patent No. 6,993,737) in view of **Rafik S. Guindi et al.** ("Design Techniques for Gate-Leakage Reduction in CMOS Circuits", 2003 IEEE, pp. 61-65).

As per **claims 3-4,6,8,10,17-20**, **Anderson et al.** disclose all of the elements of claims 1,7, as discussed in the rejections of claims 1 and 7 above. However, **Anderson et al.** failed to teach the leakage effects by taking into account of transistor stacking effects, including the particular positions within the stacks based on signals that are expected or likely to be high or low. **Rafik S. Guindi et al.** disclose design techniques for gate-leakage reduction in CMOS circuits which include taking into account of transistor stacking effects, including the particular positions within the stacks based on signals that are expected or likely (i.e., probability) to be high or low (see especially sections 5, 3.2 and 4.1; abstract). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the design techniques for gate-leakage reduction of **Rafik S. Guindi et al.** into the method/system of **Anderson et al.** because such incorporation would further reduce power consumption of the logic design being implemented on the programmable logic devices as intended by **Anderson et al.** by further taking into consideration the signals probability and transistor stacking effects as further taught by **Rafik S. Guindi et al.**.

As per **claims 11-12, Anderson et al.** in view of **Rafik S. Guindi et al.** disclose all of the elements of claim 10, from which the claims depend, as discussed above, wherein the information which includes information that the first signal is high more often than the second signal is further taught by **Rafik S. Guindi et al.** as part of the importance of signal probability (i.e., the first signal being high more often than the second signal) being used to determine the particular positions or configurations or assignments of the transistors being selected (see section 5, items 4 and 5), and is also taught by **Anderson et al.** (see Fig. 3; col. 2, lines 30-59).

7. **Claims 9,15** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Anderson et al.** (U.S. Patent No. 6,993,737) in view of **Dangelo et al.** (U.S. patent No. 6,324,678).

As per **claims 9,15**, **Anderson et al.** disclose all of the elements of claims 7 and 14, from which the respective claims depend, including the power optimization due to leakage power being performed during the design phase or after synthesis of the design (col. 8, lines 1-9). However, **Anderson et al.** failed to specifically teach the plurality of constraints that need to be balanced in addition to the power constraint, including satisfying the minimum desired clock speed constraint while reducing power consumption due to gate leakage effects. **Dangelo et al.** disclose various constraints for circuit designing to meet or minimize power (col. 36, line 35 to co. 40, line 16; Figs. 2-4) while meeting other design constraints, including using and balancing (i.e., trade-offs) various design constraints (see col. 38, lines 52-60; col. 39, lines 20-40; col. 40, lines 54-67). It would have been obvious to one of ordinary skilled in the art at the time

of the invention to further incorporate the various constraints as taught by **Dangelo et al.** into the method/system of **Anderson et al.** because such incorporation would ensure the power is optimized as taught by **Anderson et al.** while other circuit constraints are met and optimized as further taught by **Dangelo et al.**.

***Remarks***

8. The objections of **claims 1-6,18-21** due to the noted informalities are withdrawn in light of Applicant's amendment file don 2/9/2006, which corrected the informalities.

9. The rejections of **claims 1-2,5,7,9,13,21** under 35 U.S.C. 102(e) as being anticipated by **Hart et al.** (U.S. Patent Application No. 2004/0216074) are withdrawn in light of Applicant's arguments filed on 2/9/2006, wherein as pointed out by Applicant, the power consumption caused by the well biased voltage is not equivalent to the leakage gate effects as claimed. However, as given above, **Anderson et al.** (U.S. Patent No. 6,993,737) teach all of the elements of the claims.

10. The rejections of **claims 3-4,6,8,10-12,14-20** under 35 U.S.C. 103(a) as being unpatentable over **Hart et al.** (U.S. Patent Application No. 2004/0216074) in view of **Rafik S. Guindi et al.** ("Design Techniques for Gate-Leakage Reduction in CMOS Circuits", 2003 IEEE, pp. 61-65) are withdrawn in light of Applicant's arguments filed on 2/9/2006, wherein as pointed out by Applicant, **Hart et al.** failed to teach or suggest the power consumption caused by the well biased voltage is not equivalent to the leakage gate effects as claimed. However, as given in the above new rejections, **Anderson et al.** (U.S. Patent No. 6,993,737) in view of **Rafik S. Guindi et al.** ("Design Techniques for Gate-Leakage Reduction in CMOS Circuits", 2003 IEEE, pp. 61-65) teach all of the

elements of the claims, wherein the teaching of **Rafik S. Guindi et al.** is also applicable the claims for the reasons given above.

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is requested herein to consider them carefully in response to this Office Action. In particular the following prior arts made of record are most relevant:

U.S. Patent Nos.:

6,324,678, especially col. 36, line 35 to col. 40, line 16; Figs. 2-4;

6,038,386, especially col. 2, line 39 to col. 3, line 3;

5,712,790, especially col. 2, line 56 to col. 3, line 12;

6,345,379, especially col. 17, lines 53-67; col. 10, line 15 to col. 11, lie 25; col. 13, lines 21-31.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Thursday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Any response to this action should be mailed to:**

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

**or faxed to:**

571-273-8300

Phallaka Kik
U.S. Patent Examiner
March 23, 2006